Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1-2 Canceled

3. (Currently amended) A method for self-routing a plurality of packets through a $2^n \times 2^n$ switch, the switch having 2^n external input ports and 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1 b_2 ... b_n$, and composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by ~~the~~ a guide $\gamma(1), \gamma(2), ... , \gamma(k)$ where γ is a mapping from the set $\{1, 2, ... , k\}$ to the set $\{1, 2, ... , n\}$, each of the packets destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1, Q_2, ... , Q_n$, where each Q_j is a quaternary symbol in any one of the three values: '0-bound', '1-bound', and 'bicast', wherein each of the switching cells is a sorting cell associated with the partial order "'0-bound' $\prec$ 'bicast' $\prec$ '1-bound'", the method comprising:

generating a routing tag $Q_{\gamma(1)} Q_{\gamma(2)} ... Q_{\gamma(k)}$ for each of the packets ~~with reference to~~ based on the guide of the bit-permuting network and the destination output addresses of the packet, and

routing each of the packets through the network by using $Q_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the packet.

4. (Previously presented) The method as recited in claim 3 wherein each quaternary symbol is coded by two bits, where the values '0-bound', '1-bound', and 'bicast' are coded as '10', '11', and '01', respectively.

5. (Previously presented) The method as recited in claim 3 wherein the routing includes

removing the quaternary symbol $Q_{\gamma(j)}$ from the routing tag of each of the packets or rotating the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets to the end of the routing tag, before the said each of the packets exits from the j-th stage cell, $1 \leq j \leq k$, such that the leading quaternary symbol of the routing tag of the said each of the packets in the j-th stage cell, $1 \leq j \leq k$, is always $Q_{\gamma(j)}$.

6. (Previously presented) The method as recited in claim 5 wherein the routing includes using the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the said each of the packets.

7. (Previously presented) The method as recited in claim 3 wherein the switch is composed of a plurality of switching cells interconnected into a n-stage banyan-type network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(n)$ where γ is a permutation on the integers from 1 to n, and wherein the generating of a routing tag includes generating $Q_{\gamma(1)}Q_{\gamma(2)}\ldots Q_{\gamma(n)}$.

8. (Currently amended) The method as recited in claim 3 wherein the packets are classified into a number of priority classes, wherein each of the priority classes is coded as a priority code, the generating a routing tag for each of the packets includes embedding the priority code representing the priority class said each of the packets belongs to in the routing tag of the said each of the packets, and the routing includes using the priority code as ~~the~~ a tiebreaker when the two packets received at the same sorting cell are both 0-bound or both 1-bound.

9. (Previously presented) The method as recited in claim 8 wherein the packets are classified into 2^r priority classes, $r \geq 1$, where each of the priority classes is coded in an r-bit string $p_1\ldots p_r$, the generating a routing tag for the packet includes generating $Q_{\gamma(1)}p_1\ldots p_rQ_{\gamma(2)}\ldots Q_{\gamma(k)}$ as the routing tag, and the routing includes using the priority code $p_1\ldots p_r$ as the tiebreaker when the two packets received at the same sorting cell are both 0-bound or both 1-bound.

10. (Previously presented) The method as recited in claim 9 wherein the routing includes removing the quaternary symbol $Q_{\gamma(j)}$ from the routing tag of each of the packets or rotating the

leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets to the end of the routing tag, and rotating the r-bit priority code $p_1...p_r$ to the position behind the next quaternary symbol originally following the priority code in the routing tag, before said each of the packets exits from the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag of said each of the packets in the j-th stage cell, $1 \leq j < k$, are always $Q_{\gamma(j)}p_1...p_r$.

11. (Previously presented) The method as recited in claim 10 wherein the routing includes using the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets in the j-th stage cell, $1 \leq j \leq k$, and using the ensuing priority code $p_1...p_r$ as the tiebreaker when the two packets received at the same sorting cell are both 0-bound or both 1-bound, to select an output or both outputs from the j-th stage cell to emit said each of the packets.

12. (Currently amended) A method for self-routing a plurality of real data packets through a $2^n \times 2^n$ switch, the switch having (a) 2^n external input ports, (b) 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1b_2...b_n$, (c) a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by ~~the~~ <u>a</u> guide $\gamma(1), \gamma(2), ... , \gamma(k)$ where γ is a mapping from the set $\{1, 2, ... , k\}$ to the set $\{1, 2, ... , n\}$, wherein each one of the switching cells is a sorting cell associated with the partial order "'0-bound' $\prec$ 'idle' $\prec$ '1-bound' and '0-bound' $\prec$ 'bicast' $\prec$ '1-bound'", and (d) extra circuitry at the output end of each one of the switching cells, where the extra circuitry is composed of two parallel 1x1 switching elements, one at each one of the two output ports of the said each one of the switching cells, each one of the real data packets arriving at a distinct external input port determining an active input port and destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1, Q_2, ... , Q_n$, where each Q_j is a quaternary symbol in any one of the three values: '0-bound', '1-bound', and 'bicast', the method comprising<u>:</u>

generating an idle packet, which has no pre-determined destination output addresses, as a stream of '0' bits at each one of the non-active external input ports,

generating a routing tag $Q_{\gamma(1)}Q_{\gamma(2)}...Q_{\gamma(k)}$ for each one of the packets ~~with reference to~~ <u>based on</u> the guide of the bit-permuting network and the destination output addresses of the packet, wherein each $Q_{\gamma(j)}$ has one of the values of '0-bound', '1-bound', or 'bicast' for a real data packet, or has the value 'idle' for an idle packet,

routing each one of the packets through the network by using $Q_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the packet, and

processing the routing tag of each one of the packets by the extra circuitry at the output end of the j-th stage sorting cell before the said each one of the packets exiting from the said j-th stage cell by removing the leading quaternary symbol from the routing tag or rotating the leading quaternary symbol to the end of the routing tag such that the leading quaternary symbol of the routing tag of each one of the packets at each one of the j-th stage cells, $1 \leq j \leq k$, is always $Q_{\gamma(j)}$.

13. (Previously presented) The method as recited in claim 12 wherein the routing includes routing the real data packets and the idle packets through the network by sorting the packets by the sorting cells of the network, wherein the sorting at each one of the sorting cells is with respect to the partial order associated with said each one of the sorting cells and is based upon the leading quaternary symbol of the routing tag of each one of the two packets received at the cell.

14. (Previously presented) The method as recited in claim 12 wherein each quaternary symbol is coded by two bits, where the values '0-bound', '1-bound', 'idle', and 'bicast' are coded as '10', '11', '00', and '01', respectively.

15. (Previously presented) The method as recited in claim 12 wherein the switch is composed of a plurality of switching cells interconnected into a n-stage banyan-type network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(n)$ where γ is a permutation on the integers from 1 to n, and wherein the generating of a routing tag includes generating $Q_{\gamma(1)}Q_{\gamma(2)}\ldots Q_{\gamma(n)}$.

16. (Currently amended) The method as recited in claim 12 wherein the packets are classified into 2^r priority classes, $r \geq 1$, where each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the generating of routing tag for the packet includes generating $Q_{\gamma(1)}p_1 \ldots p_r Q_{\gamma(2)} \ldots Q_{\gamma(k)}$ as the routing tag, and the processing of the routing tag includes removing the quaternary symbol $Q_{\gamma(j)}$ from the routing tag of each of the packets or rotating the leading quaternary symbol $Q_{\gamma(j)}$ of

the routing tag of each of the packets to the end of the routing tag, and rotating the r-bit priority code $p_1...p_r$ to the position behind the next quaternary symbol originally following the priority code in the routing tag, before the said each of the packets exiting from the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag of the said each of the packets in the j-th stage cell, $1 \leq j \leq k$, are always $Q_{\gamma(j)}p_1...p_r$, and the routing includes using the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets in the j-th stage cell, $1 \leq j \leq k$, and using the ensuing priority code $p_1...p_r$ as ~~the~~ a tiebreaker when the two packets arrived at the same sorting cell are both 0-bound or both 1-bound, to select an output or both outputs from the j-th stage cell to emit the said each of the packets.

17. (Currently amended) A $2^n \times 2^n$ self-routing switch comprising:

an array of 2^n external input ports and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1b_2...b_n$ for routing a packet, the packet being either a real data packet destined for a rectangular set of output addresses represented by a quaternary sequence Q_1, Q_2, ... , Q_n, where each Q_j is a quaternary symbol having one of the values of '0-bound', '1-bound' or 'bicast', or being an idle packet having no pre-determined destination output address,

a switching fabric having a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by ~~the~~ a guide $\gamma(1), \gamma(2), ... , \gamma(k)$, where γ is a mapping from the set $\{1, 2, ... , k\}$ to the set $\{1, 2, ... , n\}$,

routing tag circuitry, coupled to the external input ports, for generating a routing tag $Q_{\gamma(1)}Q_{\gamma(2)}...Q_{\gamma(k)}$ for the packet ~~with reference to~~ based on the guide of the bit-permuting network and the destination addresses of the packet, and

routing control circuitry, coupled to the switching cells, for routing the packet through the switch by using $Q_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the packet.

18. (Previously presented) The system as recited in claim 17 wherein each quaternary symbol is coded by two bits, and wherein the values '0-bound', '1-bound', and 'bicast' are coded as '10', '11', and '01', respectively.

19. (Previously presented) The system as recited in claim 17 wherein the routing control circuitry includes means for removing the quaternary symbol $Q_{\gamma(j)}$ from the routing tag of each of the packets or rotating the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets to the end of the routing tag, before the said each of the packets exits from the j-th stage cell, $1 \leq j \leq k$, such that the leading quaternary symbol of the routing tag of the said each of the packets in the j-th stage cell, $1 \leq j \leq k$, is always $Q_{\gamma(j)}$.

20. (Previously presented) The system as recited in claim 19 wherein the routing control circuitry includes means for processing the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the j-th stage cell to emit the said each of the packets.

21. (Previously presented) The system as recited in claim 17 wherein the switch is composed of a plurality of switching cells interconnected into a n-stage banyan-type network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(n)$ wherein γ is a permutation on the integers from 1 to n, and wherein the routing tag circuitry includes means for generating $Q_{\gamma(1)}Q_{\gamma(2)} \ldots Q_{\gamma(n)}$.

22. (Currently amended) The system as recited in claim 17 wherein the packets are classified into 2^r priority classes, $r \geq 1$, where each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, the routing tag circuitry includes means for generating $Q_{\gamma(1)}p_1 \ldots p_r Q_{\gamma(2)} \ldots Q_{\gamma(k)}$ as the routing tag, and the routing control circuitry includes means for processing the priority code $p_1 \ldots p_r$ as ~~the~~ a tiebreaker when the two packets arrived at the same sorting cell are both 0-bound or both 1-bound.

23. (Previously presented) The system as recited in claim 22 wherein the routing control circuitry includes means for removing the quaternary symbol $Q_{\gamma(j)}$ from the routing tag of each of the packets or rotating the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets to the end of the routing tag, and rotating the r-bit priority code $p_1 \ldots p_r$ to the position behind the next quaternary symbol originally following the priority code in the routing tag, before the said each of the packets exits from the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag of the said each of the packets in the j-th stage cell, $1 \leq j \leq k$, are always

$Q_{\gamma(j)}p_1...p_r.$

24. (Previously presented) The system as recited in claim 23 wherein the routing control circuitry includes means for processing the leading quaternary symbol $Q_{\gamma(j)}$ of the routing tag of each of the packets in the j-th stage cell, $1 \leq j \leq k$, and means for processing the ensuing priority code $p_1...p_r$ as the tiebreaker when the two packets arrived at the same sorting cell are both 0-bound or both 1-bound, to select an output or both outputs from the j-th stage cell to emit the said each of the packets.

25. (Currently amended) The method as recited in claim 6 wherein the routing includes, whenever $\gamma(p) = \gamma(q)$ in the guide of the network, where $\underline{1 \leq p \leq k, 1 \leq q \leq k,}$ p<q, disabling the bicasting function of the whole stage at either stage~p or stage-q.